



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,656	09/19/2003	Thomas Vaughn	1026-0038	4630
7590	12/13/2004		EXAMINER	
Cook, Alex, McFarron, Manzo, Cummings & Mehler Suite 2850 200 West Adams Chicago, IL 60606			BENSON, WALTER	
			ART UNIT	PAPER NUMBER
			2858	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/664,656	VAUGHN ET AL.
Examiner	Art Unit	
Walter Benson	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on IDS filed 12/23/03.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-24 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1,2,4-14 and 16-24 is/are rejected.

7) Claim(s) 3 and 15 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 19 September 2003 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/23/03.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .
5) Notice of Informal Patent Application (PTO-152)
6) Other: ____ .

DETAILED ACTION

1. Claims 1-24 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 4-10, 12, 13, 16-22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over St-Germain et al. (US Patent No. 6,762,563 B2 and St-Germain hereinafter) in view of Huelson et al. (US 2004/0227708 and Huelson hereinafter).

4. As to claims 1 and 13, St-Germain discloses a system for controlling power to light emitting diodes in signaling apparatus [col. 1, lines 26-31] substantially as claimed, the system comprising:

a plurality of light emitting diodes (col. 3, lines 54-55);

a plurality of current sources for supplying current to each of the light emitting diodes with a separate current source associated with each of the plurality of light emitting diodes (col. 3, lines 57-61);

a data processor with a bus for receiving and sending data, the data processor in communication with the current sources for controlling the amount of current supplied by each current source (col. 4, lines 27-28);

a plurality resistors in series between the plurality of current sources and the plurality of light emitting diodes (col. 9, lines 53-55);

St-Germain does not expressly disclose:

a first analog-to-digital converter for determining the voltage potential at each of the plurality of resistors and for providing a digital representation of each determined voltage potential to the data processor [claims 1, 13];

the data processor using the digital representations of each determined voltage potential to control the amount of current supplied by each current source to its associated light emitting diode [claims 1, 13];

an energy storage and limiter circuit for receiving and storing input power and for supplying power to the data processor in the absence of normal input power [claims 5, 17];

where the data processor controls the plurality of current sources to provide a plurality of different current levels to each light emitting diode and the data processor compares the digital representations of the voltage received from the second analog-to-digital converter corresponding to each of the plurality of different current levels to a diode voltage-current characteristic stored in memory of the data processor [claims 9, 21];

where the data processor sequentially tests each light emitting diode by sequentially controlling the plurality of current sources to provide the plurality of different current levels to each light emitting diode [claims 10, 22].

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by St-Germain, as evidenced by Huelson.

In an analogous art, Huelson discloses a system for testing light emitting diodes having:
a first analog-to-digital converter for determining the voltage potential at each of the plurality of resistors and for providing a digital representation of each determined voltage potential to the data processor [claims 1, 13] ([0030], lines 6-9) to provide digital representation of the analog values;

the data processor using the digital representations of each determined voltage potential to control the amount of current supplied by each current source to its associated light emitting diode [claims 1, 13] ([0039], lines 11-16) to provide for remote control;

an energy storage and limiter circuit for receiving and storing input power and for supplying power to the data processor in the absence of normal input power [claims 5, 17] ([0026], lines 10-11) for backup power to the system;

where the data processor controls the plurality of current sources to provide a plurality of different current levels to each light emitting diode and the data processor compares the digital representations of the voltage received from the second analog-to-digital converter corresponding to each of the plurality of different current levels to a diode voltage-current characteristic stored in memory of the data processor [claims 9, 21] ([0039], lines 17-21) to verify illumination of the LED segment;

where the data processor sequentially tests each light emitting diode by sequentially controlling the plurality of current sources to provide the plurality of different current levels to each light emitting diode [claims 10, 22] ([0040], lines 1-4).

Given the teaching of Huelson, a person having ordinary skill at the time of the invention would have readily recognized the desirability and advantages of modifying St-Germain by employing the well known or conventional features of monitoring LED arrays, such as disclosed by Huelson, in order to use software, hardware, firmware or any combination to monitor LEDs and for the purposes discussed above.

5. As to claims 4 and 16, St-Germain discloses a system for controlling power to light emitting diodes in signaling apparatus comprising:

a pulse-width modulator coupled to a source of power and to said plurality of current sources, said pulse-width modulator in communication with said data processor to control the amount of power supplied to the plurality of current sources (col. 9, lines 41-47).

6. As to claims 6 and 18, St-Germain discloses a system for controlling power to light emitting diodes in signaling apparatus comprising:

a vital disconnect for disconnecting the system from the source to emulate an open circuit (col. 6, lines 46-51).

7. As to claims 7 and 19, St-Germain discloses a system for controlling power to light emitting diodes in signaling apparatus comprising:

a vital load circuit to emulate the load drawn by an incandescent lamp (col. 7, lines 27-30).

8. As to claims 8 and 20, St-Germain discloses a system for controlling power to light emitting diodes in signaling apparatus comprising:

where the vital load circuit draws sufficient current to satisfy hot filament tests (col. 2, lines 41-45).

9. As to claims 12 and 24, St-Germain discloses a system for controlling power to light emitting diodes in signaling apparatus comprising:

where the data processor causes the system to be vitally disconnected from the source it is determined that a predetermined number of light emitting diodes do not pass the test of comparing the voltages at the light emitting diodes to the stored diode voltage-current with claim defined in accordance characteristic (col. 6, lines 18-23).

10. Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over St-Germain in view of Huelson as applied to claims 1, 13 above, and further in view of Boerger et al. (US Patent No. 6,760,124 B1 and Boerger hereinafter).

Although the combine teaching of St-Germain and Huelson shows substantial features of the claimed invention (discussed in the paragraphs above), it fails to disclose:

a second analog-to-digital converter for determining the voltage potential of each of the plurality of light emitting diodes and for providing a digital representation of the voltage potential at each light emitting diode to the data processor;

the data processor using at the digital representation of the voltage potential at each light emitting diode to determine the junction temperature of each light emitting diode to control the

amount of current supplied by each current source to its associated light emitting diode to control the junction temperature thereof.

In an analogous art, Boerger discloses a system to determine the junction temperature of an LED having:

a second analog-to-digital converter for determining the voltage potential of each of the plurality of light emitting diodes and for providing a digital representation of the voltage potential at each light emitting diode to the data processor (col. 2, lines 15-16);

the data processor using at the digital representation of the voltage potential at each light emitting diode to determine the junction temperature of each light emitting diode to control the amount of current supplied by each current source to its associated light emitting diode to control the junction temperature thereof (col. 2, lines 29-35).

Given the teaching of Boerger, a person having ordinary skill at the time of the invention would have readily recognized the desirability and advantages of modifying St-Germain in view of Huelson by employing the well known or conventional features of monitoring LED arrays, such as disclosed by Boerger, in order to determine the illumination level and operational status of the LED.

11. Claims 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over St-Germain in view of Huelson as applied to claims 1, 13 above, and further in view of Mollet et al. (US Patent No. 6,392,553 B1 and Mollet hereinafter).

Although the combine teaching of St-Germain and Huelson shows substantial features of the claimed invention (discussed in the paragraphs above), it fails to disclose:

where the testing of each light emitting diode is performed sufficiently rapidly to avoid the human perception of a loss of illumination from the light emitting diodes.

In an analogous art, Mollet discloses a system for interfacing railway controllers with light units having:

where the testing of each light emitting diode is performed sufficiently rapidly to avoid the human perception of a loss of illumination from the light emitting diodes (col. 1, lines 54-60)

Given the teaching of Mollet, a person having ordinary skill at the time of the invention would have readily recognized the desirability and advantages of modifying St-Germain in view of Huelson by employing the well known or conventional features of monitoring LED arrays, such as disclosed by Mollet, in order to determine the operational status of the LED and avoiding any undesirable blinking of the non-incandescent light units.

Allowable Subject Matter

12. Claims 3 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record fails to teach in combination as claimed a system for controlling power to light emitting diodes where the data processor determines the junction temperature of each light emitting diode by determining the difference between the actual forward bias voltage and the normal forward bias voltage at a known temperature and by

applying a coefficient temperature related the forward bias voltage of the light emitting diodes to the difference forward bias voltages.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter Benson whose telephone number is (571) 272-2227. The examiner can normally be reached on Mon to Fri 6:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on (571) 272-2233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter Benson
Walter Benson
Patent Examiner

December 10, 2004